AMENDMENTS TO THE CLAIMS

What is claimed is:

1. (Original) A carry look-ahead adder comprising:

a carry generation circuit, organized into M blocks, arranged to perform first logic combinations on an N-bit addend and an N-bit augend, which results in carry propagation bit values and carry kill bit values, respectively, where M and N are positive integers and M<N;

a block carry circuit arranged to perform second logic combinations on the carry kill bit values, and to perform third logic operations and fourth logic operations on the propagation bit values and the carry kill values,

the second logic combination producing at least one first-type block carry signal that transitions logic states when one or more of the carry kill bit values are in a second logic state relative to a first logic state,

the third logic combination producing at least one second-type block carry signal that transitions logic states when one or more of the carry kill bit values for the lower N/(2M) bits is in the second logic state, and

the fourth logic combination producing at least one third-type block carry signal that transitions logic states when one or more of the carry kill bit values for the upper N/(2M) bits is in the second logic state;

a bit carry circuit, having a Manchester carry chain configuration, to perform a fifth logic combination on the carry propagation bit values and the carry kill bit values which results in first bit carry signals for a case where a block carry exists in each of the M blocks and results in second carry bit signals for a case where no block carry exists;

a control circuit to generate selection-control signals based upon the block carry signals, generation of the selection-control signals not logically being controlled by clock signals; and

a summation selection circuit to select between the first bit carry signals and the second bit carry signals, to add the carry propagation bit values and the selected carry signals and accordingly to output a final sum result.

2. (Original) The carry look-ahead adder of claim 1, wherein the summation selection circuit is operable to select the first bit carry signals when the block carry signals are all in the first logic state.

3. (Original) The carry look-ahead adder of claim 2, wherein the summation selection circuit is operable to select the first carry bit signals when lower bit blocks propagate carries.

4. (Original) The carry look-ahead adder of claim 3, wherein the lower bit blocks include a first previous block located immediately lower from block in which the summation is performed and a second previous block located immediately lower from the first previous block.

5. (Original) The carry look-ahead adder of claim 1, wherein the carry generation circuit includes XOR logic to produce the carry propagation bit values and NOR logic to produce the carry kill bit values.

6. (Original) The carry look-ahead adder of claim 1, wherein the block carry circuit includes OR logic operable upon all of the carry kill bit values.

7. (Original) The carry look-ahead adder of claim 1, wherein the third logic combination satisfies the following Logic Equation:

K4 =
PH<{(N/M)-1}>PH<{(N/M)-2>...PH<{N/(2M)+1}>PH<N/(2M)>
{KH<{N/(2M)-1}> +
PH<{N/(2M)-1}>KH<{N/(2M)-2}> +
PH<{N/(2M)-1}>PH<{N/(2M)-2}>KH<{N/(2M)-3}> +
.... + PH<{N/(2M)-1}>PH<{N/(2M)-2}>...PH<1>KH<0> +
PH<{N/(2M)-1}>PH<{N/(2M)-2}>...PH<1>PH<0>}

wherein K4 is the second-type block carry signal, KH<i> is a carry kill bit value, and PH<i> is a carry propagation bit value.

8. (Currently Amended) The carry look-ahead adder of claim 1, wherein the fourth logic combination satisfies the following Logic Equation:

K8 =
KH<{(N/M)-1}> +
PH<{(N/M)-1}>KH<{(N/M)-2}> +
.... + PH<{(N/M)-1}>PH<{(N/M)-2}>...PH<{(N/(2M)+2)}>KH<{N/(2M)+1}> +
PH<{(N/M)-1}>PH<{(N/M)-2}>...PH<{(N/(2M)+1)}>KH<N/(2M)>

wherein K8 is the third-type block carry signal, KH<i> is a carry kill bit value, and PH<i> is a carry propagation bit value.[.]

9. (Currently Amended) The carry look-ahead adder of claim 1, wherein the fifth logic combination satisfies Logic Equation below:

$$C0<i> = KH<i-1> + PH<i-1>C0<i-1>$$
$$C1<i> = KH<i-1> + PH<i-1>C1<i-1>$$

wherein **i** denotes integers from 0 to (N/M-1), C1<i> denotes an ith bit of the second bit carry signals, C0<i> denotes an ith bit of the first bit carry signals, and PH<> denotes the carry propagation bit value, and KH<> denotes the carry kill bit value.[~~10.~~]

10. (Original) The carry look-ahead adder of claim 1, wherein the summation circuit includes XOR logic operable upon the selected bit carry signals and the carry propagation bit values, respectively.

11. (Currently Amended) A summation method for carry look-ahead addition performed by a carry look-ahead adder, ~~the method~~ comprising:

organizing an N-bit addend and an N-bit augend into M blocks, where N and M are positive integers and N>M;

performing first logic combinations the addend and the augend resulting in carry propagation bit values and carry kill bit values;

performing second logic combinations on the carry kill bit values resulting in at least one first-type block carry signal that transitions logic states when one or more of the carry kill bit values are in a second logic state relative to a first logic state;

performing third logic operations resulting in at least one second-type block carry signal that transitions logic states when one or more of the carry kill bit values for the lower N/(2M) bits is in the second logic state, and

performing fourth logic operations on the propagation bit values and the carry kill values resulting in at least one third-type block carry signal that transitions logic states when one or more of the carry kill bit values for the upper N/(2M) bits is in the second logic state;

using Manchester carry chains to perform a fifth logic combination on the carry propagation bit values and the carry kill bit values resulting in first bit carry signals for a case where a block carry exists in each of the M blocks and results in second bit carry signals for a case where no block carry exists;

generating, independently of a clock enable signal at a logical level, selection-control signals based upon the block carry signals; and

selecting between the first bit carry signals and the second bit carry signals;

adding the carry propagation bit values and the selected carry signals resulting in a final sum result; and

outputting the final sum result.

12. (Original) The summation method of claim 11, wherein the selected bit carry signals are the first bit carry signals when the block carry signals are all in the first logic state.

13. (Original) The summation method of claim 12, wherein the selected bit carry signals are the first bit carry signals when lower bit blocks propagate carries.

14. (Original) The summation method of claim 13, wherein the lower bit blocks include a first previous block located immediately lower from block in which the summation is performed and a second previous block located immediately lower from the first previous block.

15. (Original) The summation method of claim 11, wherein the performing of the first logic combination includes applying an XOR logic operation bitwise on the addend and the

augend to produce the carry propagation bit values and applying a NOR logic operation bitwise on the addend and the augend to produce the carry kill bit values.

16. (Original) The summation method of claim 11, wherein the performing of the second logic combination includes applying OR logic to all of the carry kill bit values.

17. (Original) The summation method of claim 11, wherein the third logic combination satisfies the following Logic Equation:

K4 =
PH<{(N/M)-1}>PH<{(N/M)-2>...PH<{N/(2M)+1}>PH<N/(2M)>
{KH<{N/(2M)-1}> +
PH<{N/(2M)-1}>KH<{N/(2M)-2}> +
PH<{N/(2M)-1}>PH<{N/(2M)-2}>KH<{N/(2M)-3}> +
.... + PH<{N/(2M)-1}>PH<{N/(2M)-2}>...PH<1>KH<0> +
PH<{N/(2M)-1}>PH<{N/(2M)-2}>...PH<1>PH<0>}

wherein K4 is the second-type block carry signal, KH<i> is a carry kill bit value, and PH<i> is a carry propagation bit value.

18. (Original) The summation method of claim 11, wherein the fourth logic combination satisfies Logic Equation below:

K8 =
KH<{(N/M)-1}> +
PH<{(N/M)-1}>KH<{(N/M)-2}> +
.... + PH<{(N/M)-1}>PH<{(N/M)-2}>...PH<{(N/(2M)+2)}>KH<{N/(2M)+1}> +
PH<{(N/M)-1}>PH<{(N/M)-2}>...PH<{(N/(2M)+1)}>KH<N/(2M)>

wherein K8 is the third-type block carry signal, KH<i> is a carry kill bit value, and PH<i> is a carry propagation bit value..

19. (Original) The summation method of claim 11, wherein the fifth logic combination satisfies the following Logic Equation:

$$C0<i> = KH<i-1> + PH<i-1>C0<i-1>$$
$$C1<i> = KH<i-1> + PH<i-1>C1<i-1>$$

wherein **i** denotes integers from 0 to (N/M-1), C1<i> denotes an ith bit of the second bit carry signals, C0<i> denotes an ith bit of the first bit carry signals, and PH<> denotes the carry propagation bit value, and KH<> denotes the carry kill bit value.

20. (Original) The summation method of claim 11, wherein the adding includes performing an XOR logic operation on the selected bit carries and the carry propagation bit values, respectively.

21. (New) A carry look-ahead adder, comprising:

a carry generation circuit, organized into M blocks, arranged to perform first logic combinations on an N-bit addend and an N-bit augend, which results in carry propagation bit values and carry kill bit values, respectively, where M and N are positive integers and M<N;

a block carry circuit arranged to perform second logic combinations on the carry kill bit values, and to perform third logic operations and fourth logic operations on the propagation bit values and the carry kill values,

the second logic combination producing at least one first-type block carry signal that transitions logic states when one or more of the carry kill bit values are in a second logic state relative to a first logic state,

the third logic combination producing at least one second-type block carry signal that transitions logic states when one or more of the carry kill bit values for the lower N/(2M) bits is in the second logic state, and

the fourth logic combination producing at least one third-type block carry signal that transitions logic states when one or more of the carry kill bit values for the upper N/(2M) bits is in the second logic state.

22. (New) The carry look-ahead adder of claim 21, further comprising:

a bit carry circuit, having a Manchester carry chain configuration, to perform a fifth logic combination on the carry propagation bit values and the carry kill bit values which results in first

bit carry signals for a case where a block carry exists in each of the M blocks and results in second carry bit signals for a case where no block carry exists;

a control circuit to generate selection-control signals based upon the block carry signals, generation of the selection-control signals not logically being controlled by clock signals; and

a summation selection circuit to select between the first bit carry signals and the second bit carry signals, to add the carry propagation bit values and the selected carry signals and accordingly to output a final sum result.

23. (New) A summation method for carry look-ahead addition configured to generate a final sum result and performed by a carry look-ahead adder, comprising:

organizing an N-bit addend and an N-bit augend into M blocks, where N and M are positive integers and N>M;

performing first logic combinations the addend and the augend resulting in carry propagation bit values and carry kill bit values;

performing second logic combinations on the carry kill bit values resulting in at least one first-type block carry signal that transitions logic states when one or more of the carry kill bit values are in a second logic state relative to a first logic state;

performing third logic operations resulting in at least one second-type block carry signal that transitions logic states when one or more of the carry kill bit values for the lower N/(2M) bits is in the second logic state, and

performing fourth logic operations on the propagation bit values and the carry kill values resulting in at least one third-type block carry signal that transitions logic states when one or more of the carry kill bit values for the upper N/(2M) bits is in the second logic state.

24. (New) The method of claim 23, further comprising:

using Manchester carry chains to perform a fifth logic combination on the carry propagation bit values and the carry kill bit values resulting in first bit carry signals for a case where a block carry exists in each of the M blocks and results in second bit carry signals for a case where no block carry exists;

generating, independently of a clock enable signal at a logical level, selection-control signals based upon the block carry signals; and

selecting between the first bit carry signals and the second bit carry signals;

adding the carry propagation bit values and the selected carry signals resulting in the final sum result; and

outputting the final sum result.

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END OF CLAIM LISTING